REMARKS

Claims 1-18 are pending in this application. In the Office Action, claims 8-16 were withdrawn from consideration. By this Amendment, claims 1-3 and 7 are amended, and claims 17 and 18 are added. No new matter is added.

I. The Claims Define Patentable Subject Matter

The Office Action rejects claims 1-5 and 7 under 35 U.S.C. §102(b) as being anticipated by Sakamoto, JP2000-174044. The rejection is respectfully traversed.

Sakamoto fails to disclose the step of preparing a wiring substrate having a base substrate on which are formed interconnecting lines, apart from a semiconductor chip, as recited in claims 1 and 18.

Sakamoto discloses a liquefied closure resin constituent formed into a B-staged resin by heat-treating the wafer where the liquefied closure resin constituent was applied. However, Sakamoto fails to disclose a wiring substrate having a base substrate with interconnecting lines.

Further, Sakamoto fails to disclose melting the base substrate while bumps provided on the semiconductor chip are pressed into the base substrate, as recited in claims 1 and 18.

Sakamoto discloses diced semiconductor elements bonded to a board, and at the same time, the B-staged resin composition is heat-fluidized so that the composition is cooled. However, Sakamoto fails to disclose melting the base substrate while pressing the bumps and semiconductor chip together. In fact, Sakamoto fails to disclose or even mention the process of pressing the bumps and semiconductor chip together since the thermosetting liquid sealing resin composition is B-staged. What Sakamoto teaches is creating (para. [0009] of the attached computer translation) a semi-conductor device with solder bumps and a resin that coats the semi-conductor device which is then mounted to a substrate by melting the solder bumps and the resin which flows to fill the gap between the semi-conductor device and the

substrate during application of pressure (para. [0013]). Accordingly, Sakamoto fails to disclose melting the base substrate while bumps provided on the semiconductor chip are pressed in, as recited in claims 1 and 18 as presented, in fact, teaches away from the invention.

Sakamoto also fails to disclose the electrically connecting the bumps to the interconnecting lines, as recited in claims 1 and 18.

Sakamoto merely discloses a plurality of semiconductor elements having bumps for electrical connection to the board. That is, although Sakamoto discloses bumps for electrical connection to the board, Sakamoto fails to disclose any interconnecting lines with connecting portions which are electrically connected with the bumps. By providing the substrate with interconnecting lines formed on one surface of the base substrate, it becomes simple to mount the semiconductor chip on both sides.

Because Sakamoto does not literally disclose the claimed invention, it cannot provide the basis for rejection under 35 U.S.C. §102. Thus, it is respectfully requested that the rejection be withdrawn.

The Office Action rejects claim 6 under 35 U.S.C. §103(a) as being unpatentable over Sakamoto in view of U.S. Patent 6,208,525 to Imasu et al. (hereinafter "Imasu"). The rejection is respectfully traversed.

As discussed above, Sakamoto neither discloses nor suggests the claimed invention as found in claim 1, the independent claim from which the rejected claim depends. Imasu fails to overcome the noted deficiencies of Sakamoto. It is respectfully requested that the 35 U.S.C. §103 rejection be withdrawn.

For at least these reasons, Applicant respectfully submits that Sakamoto and Imasu, individually or in combination, fail to disclose or render obvious the features recited in independent claims 1 and 18. Claims 2-7 and 17, which depend from independent claim 1 are

likewise distinguished over the applied art for at least the reasons discussed, as well as for the additional features they recite. Reconsideration and withdrawal of the rejections are respectfully requested.

II. Conclusion

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 1-18 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

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Attachment:
Translation of Japanese Patent 2000-174044

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United States Patent Application ***20020079594***
Kind Code **A1**
Sakurai, Kazunori **June 27, 2002**

Semiconductor device and method of manufacture thereof, circuit board, and electronic instrument

Abstract

A method of manufacturing a semiconductor device comprises a step of mounting a semiconductor chip on a wiring substrate having a base substrate on which are formed interconnecting lines; while melting the base substrate, bumps provided to the semiconductor chip are pressed in, and the bumps are electrically connected to the interconnecting lines.

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Dec 26, 2000	JP	2000-395111(P)

Claims

What is claimed is:

1. A method of manufacturing a semiconductor device comprising a step of mounting a semiconductor chip on a wiring substrate having a base substrate on which are formed interconnecting lines, wherein while melting the base substrate, bumps provided to the semiconductor chip are pressed in, and the bumps are electrically connected to the interconnecting lines.

2. The method of manufacturing a semiconductor device as defined in claim 1, wherein the interconnecting lines comprise connecting portions electrically connecting with the bumps, and wherein in the step of electrical connection, the base substrate is melted, and the bumps and the connecting portions are sealed with the melted material of the base substrate.

3. The method of manufacturing a semiconductor device as defined in claim 1, wherein in the step of electrical connection, the base substrate is melted, and the melted material of the base substrate is adhered closely to a surface of the semiconductor chip.

4. The method of manufacturing a semiconductor device as defined in claim 1, wherein in the step of electrical connection, the base substrate is melted by heat.

5. The method of manufacturing a semiconductor device as defined in claim 1, wherein a thermoplastic resin is used as the base substrate.

6. The method of manufacturing a semiconductor device as defined in claim 1, wherein in the step of electrical connection, the semiconductor chip is held by a jig, heat is applied to the jig to heat at least the bumps of the semiconductor chip, and the jig is pressed in the direction of the base substrate, whereby the bumps are pressed into the base substrate.

7. The method of manufacturing a semiconductor device as defined in claim 1, further comprising: a step of mounting another semiconductor chip on the wiring substrate.

8. A semiconductor device manufactured by the manufacturing method as defined in claim 1.

9. A semiconductor device comprising: a semiconductor chip having electrodes on which bumps are formed; and a wiring substrate on which the semiconductor chip is mounted, and having a base substrate on which are formed interconnecting lines having connecting portions electrically connecting to the bumps, wherein the bumps are embedded in the base substrate and electrically connected to the interconnecting lines; and wherein the bumps and the connecting portions are sealed by the base substrate.

10. The semiconductor device as defined in claim 9, wherein the base substrate is adhered closely to a surface of the semiconductor chip.

11. The semiconductor device as defined in claim 9, wherein the base substrate is a thermoplastic resin.

12. The semiconductor device as defined in claim 9, further comprising: another semiconductor chip mounted on the wiring substrate.

13. A circuit board on which the semiconductor device as defined in claim 8 is mounted.

14. A circuit board on which the semiconductor device as defined in claim 9 is mounted.

15. An electronic instrument comprising the semiconductor device as defined in claim 8.

16. An electronic instrument comprising the semiconductor device as defined in claim 9.

Description

[0001] Japanese Patent Application No. 2000-395111, filed Dec. 26, 2000, is hereby incorporated by reference in its entirety.

TECHNICAL FIELD

[0002] The present invention relates to a semiconductor device and method of manufacture thereof, a circuit board, and an electronic instrument.

BACKGROUND

[0003] As one type of CSP (Chip Scale/Size Package) semiconductor device is known the construction in which a semiconductor chip is mounted face down on a substrate (flip-chip connection).

[0004] In this case, between the semiconductor chip and the substrate a resin is commonly provide as an underfill material. The resin is provided by being injected between the semiconductor chip and the substrate after mounting, or by being previously applied to the substrate before mounting. However, the step of providing the resin entails an extra process, and makes the manufacturing process of the semiconductor device correspondingly longer.

[0005] Moreover, with the development of multi-chip modules in recent years, the configuration of mounting semiconductor chips on both surfaces of a wiring substrate has been developed. However, for this purpose, interconnecting lines must be formed on both surfaces of a substrate, and further for electrical conduction between the interconnecting lines on both surfaces via holes are required, resulting in increased costs and degraded manufacturing processes.

SUMMARY

[0006] According to the first aspect of the present invention, there is provided a method of manufacturing a semiconductor device comprising a step of mounting a semiconductor chip on a wiring substrate having a base substrate on which are formed interconnecting lines, and

[0007] while melting the base substrate, bumps provided to the semiconductor chip are pressed in, and the bumps are electrically connected to the interconnecting lines.

[0008] A semiconductor device according to the second aspect of the present invention can be manufactured by the above described manufacturing method.

[0009] A semiconductor device according to the third aspect of the present invention comprises:

[0010] a semiconductor chip having electrodes on which bumps are formed; and

[0011] a wiring substrate on which the semiconductor chip is mounted, and having a base substrate on which are formed interconnecting lines having connecting portions electrically connecting to the bumps,

[0012] wherein the bumps are embedded in the base substrate and electrically connected to the interconnecting lines; and

[0013] wherein the bumps and the connecting portions are sealed by the base substrate.

[0014] A circuit board according to the fourth aspect of the present invention has the above described semiconductor device mounted thereon.

[0015] An electronic instrument according to the fifth aspect of the present invention comprises the above described semiconductor device.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] FIGS. 1A to 1C show a first embodiment of the semiconductor device to which the present invention is applied and a method of manufacture thereof.

[0017] FIG. 2 shows a second embodiment of the semiconductor device to which the present invention is applied.

[0018] FIG. 3 shows the method of manufacture of the second embodiment of the semiconductor device to which the present invention is applied.

[0019] FIG. 4 shows a shows a first example of the third embodiment of the semiconductor device to which the present invention is applied.

[0020] FIG. 5 shows a second example of the third embodiment of the semiconductor device to which the present invention is applied.

[0021] FIG. 6 shows a third example of the third embodiment of the semiconductor device to which the present invention is applied.

[0022] FIG. 7 shows the third example of the third embodiment of the semiconductor device to which the present invention is applied.

[0023] FIG. 8 shows a fourth example of the third embodiment of the semiconductor device to which the present invention is applied.

[0024] FIG. 9 shows a circuit board on which the embodiment of the semiconductor device to which the present invention is applied is mounted.

[0025] FIG. 10 shows an electronic instrument having the embodiment of the semiconductor device to which the present invention is applied.

[0026] FIG. 11 shows an electronic instrument having the embodiment of the semiconductor device to which the present invention is applied.

DETAILED DESCRIPTION

[0027] With this embodiment, the above problems can be solved, and a semiconductor device and method of manufacture thereof allowing semiconductor chip mounting in fewer steps, a circuit board, and an electronic instrument can be provided.

[0028] (1) According to this embodiment, there is provided a method of manufacturing a semiconductor device comprising a step of mounting a semiconductor chip on a wiring substrate having a base substrate on which are formed interconnecting lines, and

[0029] while melting the base substrate, bumps provided to the semiconductor chip are pressed in, and the bumps are electrically connected to the interconnecting lines.

[0030] According to this embodiment, while melting the base substrate, the bumps provided to the semiconductor chip are pressed in, and the bumps are electrically connected to the interconnecting lines. By means of this, with for example the wiring substrate having the interconnecting lines formed on one surface of the base substrate, it is simple to mount the semiconductor chips on both sides. Also, for example, since the bumps and the like can be sealed with the melted material of the base substrate, a high reliability semiconductor device can be manufactured in a smaller number of steps.

[0031] (2) In this method of manufacture of a semiconductor device:

[0032] the interconnecting lines may comprise connecting portions electrically connecting with the bumps, and

[0033] in the step of electrical connection, the base substrate may be melted, and the bumps and the connecting portions may be sealed with the melted material of the base substrate.

[0034] By means of this, electrically connecting the bumps to the connecting portions of the interconnecting lines, and sealing them, can be carried out in a single step.

[0035] (3) In this method of manufacture of a semiconductor device:

[0036] in the step of electrical connection, the base substrate may be melted, and the melted material of the base substrate may be adhered closely to a surface of the semiconductor chip.

[0037] By means of this, since the melted material of the base substrate is adhered to the surface of the semiconductor chip, stress applied to the semiconductor chip can be absorbed by the base substrate.

[0038] (4) In this method of manufacture of a semiconductor device:

[0039] in the step of electrical connection, the base substrate may be melted by heat.

[0040] By means of this, since the base substrate can be melted by means of the heat for electrically connecting the bumps to the interconnecting lines for example, the base substrate can be melted easily.

[0041] (5) In this method of manufacture of a semiconductor device:

[0042] a thermoplastic resin may be used as the base substrate.

[0043] By means of this, further subsequent processing by heat is easy.

[0044] (6) In this method of manufacture of a semiconductor device:

[0045] in the step of electrical connection, the semiconductor chip may be held by a jig, heat may be applied to the jig to heat at least the bumps of the semiconductor chip, and the jig may be pressed in the direction of the base substrate, whereby the bumps may be pressed into the base substrate.

[0046] (7) This method of manufacture of a semiconductor device may further comprise:

[0047] a step of mounting another semiconductor chip on the wiring substrate.

[0048] (8) This embodiment of the semiconductor device can be manufactured by the above described manufacturing method.

[0049] (9) This embodiment of the semiconductor device comprises:

[0050] a semiconductor chip having electrodes on which bumps are formed; and

[0051] a wiring substrate on which the semiconductor chip is mounted, and having a base substrate on which are formed interconnecting lines having connecting portions electrically connecting to the bumps,

[0052] wherein the bumps are embedded in the base substrate and electrically connected to the interconnecting lines; and

[0053] wherein the bumps and the connecting portions are sealed by the base substrate.

[0054] According to this embodiment, since the bumps and the connecting portions are sealed by the base substrate, it is not necessarily required to provide a resin for sealing other than the wiring substrate, and the number of elements of the device can be reduced. Since the bumps are embedded in the base substrate, the semiconductor device can be made thinner.

[0055] (10) In this semiconductor device:

[0056] the base substrate may be adhered closely to a surface of the semiconductor chip.

[0057] By means of this, stress applied to the semiconductor chip can be absorbed by the base substrate.

[0058] (11) In this semiconductor device:

[0059] the base substrate may be a thermoplastic resin.

[0060] (12) This semiconductor device may further include:

[0061] another semiconductor chip mounted on the wiring substrate.

[0062] (13) This embodiment of a circuit board has the above described semiconductor device mounted thereon.

[0063] (14) This embodiment of an electronic instrument comprises the above described semiconductor device.

[0064] The present invention is now described in terms of a number of embodiments, with reference to the drawings. However, the present invention is not limited to these embodiments.

First Embodiment

[0065] FIGS. 1A to 1C show a method of manufacturing a semiconductor device of the first embodiment to which the present invention is applied. In this embodiment, a semiconductor chip 10 and a wiring substrate 20 are used.

[0066] The form of the semiconductor chip 10 may be a rectangular parallelepiped (including a cube), or may be spherical. The semiconductor chip 10 has a plurality of electrodes 12. The electrodes 12 are external electrodes of the circuit elements formed on the semiconductor chip 10, and are pads formed of thin aluminum, copper, or the like. The electrodes 12 are commonly formed on either one surface of the semiconductor chip 10. The electrodes 12 may be formed on the surface of the semiconductor chip 10 inside the active region in which the circuit elements are formed, or may be formed on the outside.

[0067] The electrodes 12 may be formed at the extremity of the surface of the semiconductor chip 10. The electrodes 12 may be formed on two parallel sides of the semiconductor chip 10, or on four sides. On the semiconductor chip 10, avoiding at least some of the electrodes 12, a passivation film (not shown in the drawings) is formed. The passivation film can be formed of, for example, SiO.sub.2, SiN, a polyimide resin, or the like.

[0068] On the electrodes 12 are provided bumps 14. The bumps 14 may be formed of at least one of gold, nickel, copper, silver, tin, and the like. The surface of the bumps 14 may be plated. The bumps 14 may be solder plated. The

form of the bumps 14 is not particularly restricted, and may be squashed flat, or may project, or may have a ball shape. The height of the bumps 14 is not particularly restricted. The bumps 14 may be formed by electroplating or electroless plating, or may be formed in a ball shape by melting a bonding wire. In the example shown in the drawings, the bumps 14 are single-step, but may equally be multiple step.

[0069] The wiring substrate 20 includes a base substrate 22, and the plurality of interconnecting lines 24 formed on the base substrate 22. The plurality of interconnecting lines 24 is supported by the base substrate 22, and may be formed, for example, on one surface of the base substrate 22. The wiring substrate 20 may be a three-layer substrate with the interconnecting lines 24 formed on the base substrate 22 with an adhesive (not shown in the drawings) interposed, or it may be a two-layer substrate in which the interconnecting lines 24 are formed on the base substrate 22 without an adhesive.

[0070] The interconnecting lines 24 refer to portions that provide electrical connection between at least two points, and the plurality of individually formed interconnecting lines 24 may be referred to as an interconnecting pattern. The interconnecting lines 24 may be formed by laminating any of copper (Cu), chromium (Cr), titanium (Ti), nickel (Ni), and titanium-tungsten (Ti--W), or may be formed of a single layer of any of these. In this case, the interconnecting lines 24 are desirably plated with solder, tin, gold, nickel, or the like. The interconnecting lines 24 can be formed by etching, plating treatment, or sputtering or the like. For example, a copper foil may be adhered to the base substrate 22 by heat and pressure, a copper pattern formed by photoetching, and then the interconnecting lines 24 formed by further plating with tin or gold or the like.

[0071] The interconnecting lines 24 have a plurality of connecting portions 26. The connecting portions 26 are parts of the interconnecting lines 24 for electrical connection to the semiconductor chip 10. The connecting portions 26 are electrically connected to the bumps 14. The connecting portions 26 may be lands. The connecting portions 26 are plated with solder or the like to enable a good connection.

[0072] The base substrate 22 is desirably formed of an organic material. The base substrate 22 is desirably formed of a material including a resin. The base substrate 22 may be of a thermoplastic resin. By means of a thermoplastic resin, after once processing as a wiring substrate 20, further subsequent processing is easy. Alternatively, the base substrate 22 may be of a thermosetting resin. Even if a thermosetting resin, if for example the interconnecting lines 24 are supported while in a semi-cured state, further subsequent processing is possible.

[0073] The base substrate 22 may be of a resin in which conducting particles (not shown in the drawings) are included. The base substrate 22 may be an anisotropic conductive film (ACF). The bumps 14 are electrically connected to the connecting portions 26 with the conducting particles interposed. If an anisotropic conductive film is used, it is electrically conducting only in the direction in which the conducting particles are squashed, and is not conducting in other directions. Therefore, even when the plurality of interconnecting lines 24 is supported by the anisotropic conductive film, the interconnecting lines 24 are not mutually electrically conducting.

[0074] As the material of the base substrate 22 may be used a liquid crystal polymer (LCP). A liquid crystal polymer exhibits a liquid crystal state when melted. Compared with other polymers, it is characterized by reduced dimensional variation due to temperature or humidity.

[0075] For example, as the wiring substrate 20 may be used a flexible copper lamination having the liquid crystal polymer film BIAC (registered trade mark) on which a copper foil (the interconnecting lines 24) is formed. By means of this, the water absorption ratio is reduced, and even under conditions of high humidity, high dimensional stability can be maintained. Furthermore, since the coefficient of linear thermal expansion is arranged to be almost the same as that of copper foil (the interconnecting lines 24), warping due to temperature variations is eliminated.

[0076] As shown in FIG. 1A, the semiconductor chip 10 opposes the base substrate 20. As shown in the drawing, when a wiring substrate 20 having interconnecting lines 24 on one surface is used, the semiconductor chip 10 opposes the other surface of the wiring substrate 20. The semiconductor chip 10 has the surface on which the electrodes 12 are formed opposing the wiring substrate 20. The semiconductor chip 10 is subjected to so-called face-down mounting.

[0077] The bumps 14 of the semiconductor chip 10 are aligned with the connecting portions 26 of the interconnecting lines 24. For example, the wiring substrate 20 may be mounted on a stage not shown in the drawings, and the semiconductor chip 10 held in a jig 30 for the alignment. The jig 30 may hold the surface of the semiconductor chip 10 opposite to the surface on which the electrodes 12 are formed by suction. In the example shown in the drawings, the jig 30 has an internal heater 32 supplying heat from a heat source.

[0078] Next, as shown in FIG. 1B, the bumps 14 of the semiconductor chip 10 are pressed into the base substrate 22 while melting the base substrate 22. To express this in a different order, the base substrate 22 is melted while pressing the bumps 14 of the semiconductor chip 10 into the base substrate 22.

[0079] For melting the base substrate 22, energy concordant with the mechanism of melting of the base substrate 22 may be applied. The energy may be radiation (including visible light, ultraviolet radiation, electron beam, X-rays, and so on), or heat or the like. In the example shown in the drawings, the base substrate 20 is melted by heat. In this case, the base substrate 22 may be heated and melted by the heater 32 of the jig 30. The heater 32 heats at least the bumps 14 of the semiconductor chip 10.

[0080] In order to press in the bumps 14 of the semiconductor chip 10, at least one of the semiconductor chip 10 and base substrate 22 is pressed against the other. For example, with the jig 30 pressed against the semiconductor chip 10, it may be pressed against the base substrate 22. If the jig 30 is used, the melting of the base substrate 22, and the pressing in of the bumps 14 of the semiconductor chip 10 can be carried out simultaneously.

[0081] In this way, as shown in FIG. 1C, the bumps 14 are pressed into the melted base substrate 22, and are electrically connected to the interconnecting lines 24. By means of this, compared with the case in which the bumps 14 are mechanically pressed into the base substrate 22 without melting the base substrate 22, the electrical connection of the bumps 14 to the interconnecting lines 24 can be achieved with the application of a lower pressure. Furthermore, by melting the base substrate 22, because the bumps 14 push aside the melted material of the base substrate 22, a more definite connection to the connecting portions 26 is achieved.

[0082] The bumps 14 and connecting portions 26 may be sealed by the base substrate 22. In more detail, on the periphery of the bumps 14 and the connecting portions 26, the melted material of the base substrate 22 is provided to be in intimate contact therewith. When the bumps 14 and connecting portions 26 are electrically connected, the melted material of the base substrate 22 flows to fill the gap on the periphery thereof. By means of this, electrical short circuits are prevented, and an improvement in the resistance of the device to moisture is implied.

[0083] The surface of the semiconductor chip 10 may be in intimate contact with the base substrate 22. That is to say, the semiconductor chip 10 may be pressed into the base substrate 22, and the melted material of the base substrate 22 may form an intimate contact with the surface of the semiconductor chip 10. In the example shown in the drawings, the semiconductor chip 10 is in intimate contact with the base substrate 22 on the surface on which the electrodes 12 are formed. It should be noted that the semiconductor chip 10 may be partially embedded in the base substrate 22, or may be not embedded.

[0084] By means of this, between the semiconductor chip 10 and the interconnecting lines 26 can be seamlessly filled with the resin or similar material of the base substrate 22. Therefore, stress concentrated on the bumps 14 (or connecting portions 26 of the interconnecting lines 24) can be distributed over the whole surface of the semiconductor chip 10 by the base substrate 22. In other words, stress applied to the semiconductor chip 10 can be absorbed by the base substrate 22.

[0085] It should be noted that the thickness of the base substrate 22 may be more than the distance in the thickness direction by which the bumps 14 project from the surface of the semiconductor chip 10 having the electrodes 12. By means of this, a part of the semiconductor chip 10 can be embedded in the base substrate 22, and the intimate contact between the semiconductor chip 10 and the base substrate 22 can be made easier to achieve.

[0086] This embodiment of the semiconductor device is now described. It should be noted that in the following

description, description which would duplicate content described in the method of manufacture is omitted.

[0087] As shown in FIG. 1C, a semiconductor device 1 includes a semiconductor chip 10 having a plurality of electrodes 12 and bumps 14 formed on the electrodes 12, and a wiring substrate 20 in which the plurality of interconnecting lines 24, having electrical connecting portions 26 with the bumps 14, are formed on the base substrate 22. In the example shown in the drawings, the interconnecting lines 24 are formed on one surface of the base substrate 22. In other words, the wiring substrate 20 has a surface on the side of the base substrate 22 and a surface on the side of the interconnecting lines 24.

[0088] In the example shown in the drawings, the semiconductor chip 10 is mounted on the surface of the wiring substrate 20 on the side of the base substrate 22. Then the bumps 14 enter the base substrate 22 and are electrically connected to the interconnecting lines 24. The bumps 14 are connected to the connecting portions 26 on the surface of the base substrate 22 opposite to that on which the semiconductor chip 10 is provided. That is to say, the bumps 14 pass through the base substrate 22. The semiconductor chip 10 is subjected to so-called face-down mounting to the interconnecting lines 24.

[0089] The bumps 14 and connecting portions 26 are sealed by the base substrate 22. That is to say, both are in intimate contact with the solidified material of the base substrate 22. The base substrate 22 may be in intimate contact with the surface of the semiconductor chip 10 having the electrodes 12. In the example shown in the drawings, the surface of the base substrate 22 is flat outside the area in which the semiconductor chip 10 is provided, but in addition may be raised so as to cover at least a part of the extremity of the semiconductor chip 10.

[0090] By means of this, the bumps 14 and connecting portions 26 are sealed by the base substrate 22, and therefore it is not necessarily required to provide a sealing resin separate from the wiring substrate 20, and the number of components in the device is reduced. Since the bumps 14 enter the base substrate 22, the semiconductor device can be made thinner.

[0091] It should be noted that the package form of this embodiment of the semiconductor device may be termed a BGA (Ball Grid Array) or CSP (Chip Size/Scale Package). As the wiring substrate 20, a COF (Chip On Flex/Film) substrate or COB (Chip On Board) substrate may be used.

Second Embodiment

[0092] FIGS. 2 and 3 show a second embodiment of the semiconductor device to which the present invention is applied. In this embodiment, an example of a semiconductor device and method of manufacture thereof is described, in which the mounting configuration of the above described semiconductor chip is applied to a multi-chip module configuration. It should be noted that in the following description, as far as possible, content described in the first embodiment can be applied.

[0093] A semiconductor device 2 includes first and second semiconductor chips 10 and 40, and a wiring substrate 20. The first semiconductor chip 10 is as already described, and the second semiconductor chip 40 has a plurality of electrodes 42, and on the electrodes 12 are formed bumps 44. In the example shown in the drawing, the wiring substrate 20 has interconnecting lines 24 formed on one surface of the base substrate 22.

[0094] The second semiconductor chip 40 is subjected to face-down mounting on the surface of the wiring substrate 20 on the side of the interconnecting lines 24. As for example shown in FIG. 2, the second semiconductor chip 40 may be adhered to the wiring substrate 20 with an anisotropic conducting material 50 including conducting particles 52 interposed. In this case, the bumps 44 are electrically connected to the interconnecting lines 24 through the conducting particles 52.

[0095] The second semiconductor chip 40 may be a "mirror chip" of the first semiconductor chip 10. Also, the bumps 44 may be connected to the connecting portions 26 to which the bumps 14 of the first semiconductor chip 10 are electrically connected.

[0096] By means of this, for example, when the first and second semiconductor chips 10 and 40 are memory, from the same arrangement of external terminals (not shown in the drawings), data can be read out from or written to the memory cell at the same address in each memory. Furthermore, for the first and second semiconductor chips 10 and 40, by separating only the chip select terminal connections, the same external terminal arrangement can be used, and at least two (a plurality is possible) semiconductor chips can be separately controlled.

[0097] According to this embodiment of the semiconductor device, since the second semiconductor chip 40 is mounted on the surface on which the interconnecting lines 24 are formed, the semiconductor chips 10 and 40 can be simply mounted on both surfaces. Furthermore, the first semiconductor chip 10 has the bumps 14 embedded in the base substrate 22, and therefore the semiconductor device 2 can be made thinner. Therefore, a low-cost and compact multi-chip module can be provided.

[0098] FIG. 3 shows a method of manufacture of this embodiment of the semiconductor device. The first and second semiconductor chips 10 and 40 may be separately mounted on the wiring substrate 20, or may be mounted approximately simultaneously.

[0099] If the first and second semiconductor chips 10 and 40 are mounted approximately simultaneously, since pressure can be applied from both sides of the connecting portions 26 of the interconnecting lines 24, the process can be completed without applying excessive stress to the interconnecting lines 24. If the mounting is simultaneous, the mounting time can be reduced, and therefore the manufacturing efficiency is increased.

[0100] When the first and second semiconductor chips 10 and 40 are mounted separately, the first semiconductor chip 10 may be mounted first. If this is done, the second semiconductor chip 40 can be mounted after confirming the connection of the bumps 14 to the connecting portions 26, and therefore the occurrence of faults can be reduced.

Third Embodiment

[0101] FIGS. 4 to 8 show the third embodiment of the semiconductor device to which the present invention is applied. In this embodiment, a semiconductor device is shown in which the semiconductor chip mounting configuration shown in the first embodiment is applied to a multi-chip module configuration. It should be noted that in the following description, as far as possible, content described in the above described embodiments can be applied.

FIRST EXAMPLE

[0102] FIG. 4 shows a first example of this embodiment of the semiconductor device. A semiconductor device 3 includes first and second semiconductor chips 10 and 60, and a wiring substrate 20. In the first example, the difference from the example shown in the second embodiment is that the external forms of the first and second semiconductor chips 10 and 60 are different from each other.

[0103] The second semiconductor chip 60 may be larger in outline than the first semiconductor chip 10, or may be smaller. Bumps 64 on electrodes 62 are electrically connected to the interconnecting lines 24 by connecting portions 28 in positions different from those of the connecting portions 26 connecting to the first bumps 14 of the semiconductor chip 10.

[0104] In the example shown in the drawings, the external terminals of the wiring substrate 20 are omitted. The external terminals are connected to circuit elements (for example a liquid crystal panel or motherboard), not shown in the drawings. For example, a part of the wiring substrate may be extended, to form external connections. That is to say, part of the interconnecting lines 24 supported on the base substrate 22 may be connector leads.

SECOND EXAMPLE

[0105] FIG. 5 shows a second example of this embodiment of the semiconductor device. A semiconductor device 4 includes first and second semiconductor chips 10 and 70, and the second semiconductor chip 70 is sealed with a resin

76.

[0106] The second semiconductor chip 70 is mounted face up on the wiring substrate 20. Electrodes 72 are connected to the connecting portions 28 with wires 74 interposed. The resin 76 may be a molding resin that can be used with a die. It should be noted that in the example shown in the drawing again, the external terminals of the wiring substrate 20 are omitted.

THIRD EXAMPLE

[0107] FIGS. 6 and 7 show a third example of this embodiment of the semiconductor device. A semiconductor device 5 includes first and second semiconductor chips 10 and 40 and a wiring substrate 20. On the wiring substrate 20 is provided a plurality of solder balls 80 as external terminals.

[0108] The wiring substrate 20 has a region in which the first and second semiconductor chips 10 and 40 are mounted, and a region in which the plurality of solder balls 80 is provided. By providing the regions separately, stresses applied to the semiconductor chip or the like during the manufacturing process can be limited. The mounting region of the semiconductor chips and the mounting region of the solder balls 80 may be of approximately the same size. By virtue of this, the two regions may be overlaid.

[0109] It should be noted that for a single region in which the solder balls 80 are provided, two or more semiconductor chip mounting regions may be provided. By folding the regions in which the semiconductor chips are mounted from a plurality of directions, a semiconductor device can be manufactured with approximately the same plan area as the region in which the solder balls 80 are provided.

[0110] The solder balls 80 may, as shown in the drawing project from the base substrate 22 side of the wiring substrate 20, or may project from the interconnecting lines 22 side of the wiring substrate 20. In the case of projecting on the base substrate 22 side, the solder balls 80 project through penetrating holes 23 in the base substrate 22. The penetrating holes 23 are formed in a portion overlying the interconnecting lines 24. The solder balls 80 can be provided by disposing preformed solder on lands 25 which are a portion of the interconnecting lines 24, and forming in a reflow process.

[0111] Alternatively, without explicitly providing balls, the solder balls 80 may be provided by applying solder to the circuit elements. The semiconductor chip (not shown in the drawings) may be mounted in the region in which the solder balls 80 are provided.

[0112] A semiconductor device 6 shown in FIG. 7 has a semiconductor device 5 in folded form. In more detail, the regions in which the semiconductor chips 10 and 40 are mounted are overlaid in such a way that in the region in which solder balls 80 are provided, the solder balls 80 project to the outside. By means of this, a compact and high density semiconductor device can be provided.

FOURTH EXAMPLE

[0113] FIG. 8 shows a fourth example of this embodiment of the semiconductor device. A semiconductor device 7 has a part of the interconnecting lines 24 in a bent portion 90, constituting a plurality of external terminals.

[0114] The bent portion 90 projects from the surface of the base substrate 22. In more detail, the interconnecting lines 24 have their ends in the direction of projecting from the base substrate 22 bent. In the base substrate 22 in the position of the bent portion 90, penetrating holes 92 may be formed. By means of this, for example a convex form jig can be passed through the penetrating holes 92 to form the convex bent portion 90 in the interconnecting lines 24.

[0115] In FIG. 8, the bent portion 90 projects from the wiring substrate 20 on the side of the interconnecting lines 24, but it may equally project through the penetrating holes 92 from the side of the base substrate 22. Since the external terminals are constituted using a portion of the interconnecting lines 24, the number of components of the semiconductor device can be reduced.

[0116] The bent portion 90 may be formed by a central portion of a part of the interconnecting lines 24 (for example lands) projecting. In this case, the inside of the bent portion 90 may be filled with conducting paste or the like. Since the external terminals are formed of the interconnecting lines 24 (for example copper) which are harder than solder, the temperature cycle reliability of the device is improved.

[0117] It should be noted that this example can be applied to replace the solder balls 80 in all embodiments having the above described solder balls 80.

[0118] According to the configuration of the above described multi-chip module, since the first semiconductor chip 10 is mounted on the side of the wiring substrate 20 of the base substrate 22, another semiconductor chip (the second semiconductor chip 60 or 70) can be mounted on the side on which the interconnecting lines 24 are formed, in a variety of configurations, and in a simple way. Moreover, the bumps 14 of the semiconductor chip 10 are embedded in the base substrate 22, and therefore the semiconductor device can be made more compact. Other benefits are as described for the above described embodiments.

[0119] FIG. 9 shows an embodiment of a circuit board to which the present invention is applied. As shown in FIG. 9, the above described semiconductor device is electrically connected to the circuit board. The circuit board may, for example, be a liquid crystal panel 100. The semiconductor device 1 has the form of stamping out the outline surrounding the plurality of interconnecting lines 24 in the base substrate 22 of a tape form semiconductor device.

[0120] As an electronic instrument having the semiconductor device to which the present invention is applied, in FIG. 10 is shown a notebook personal computer 200. In FIG. 11, is shown a mobile telephone 300. This mobile telephone 300 has the circuit board (liquid crystal panel 100) to which the present invention is applied.

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